LOW GATE RESISTANCE LAYOUT PROCEDURE FOR RF TRANSISTOR DEVICES

ABSTRACT

A region on a substrate contains multiple transistors in parallel that share a single salicided polysilicon gate electrode. Above or below the gate electrode are formed multiple plugs of refractory material along the length of the gate electrode. The multiple plugs of refractory material electrically interconnect the gate signal line and the salicided polysilicon gate electrode. The plug material is selected to minimize the work function between it and the salicided polysilicon gate electrode.